REMARKS

In the Official Action mailed 25 February 2005, the Examiner objected to paragraph [0001] of the specification for informalities. The Examiner reviewed claims 1-48. The Examiner has rejected claims 1-3, 6-17, 22-33 and 38-48 under 35 U.S.C. §102(e); and has objected to claims 2-6, 18-21 and 34-37 as being dependent upon a rejected base claim.

The Examiner's objection and rejection are respectfully traversed below.

Objection to the Specification

The Examiner has objected to paragraph [0001] of the specification because the serial number for a commonly owned U.S. Patent Application is missing. Paragraph [0001] of the specification is amended herein to add the serial number.

Accordingly, reconsideration of the objection to the specification as amended is respectfully requested.

Rejection of Claims 1-3, 6-17, 22-33 and 38-48 under 35 U.S.C. §102(e)

The Examiner has rejected claims 1-3, 6-17, 22-33 and 38-48 (including independent claims 1, 17 and 33) under 35 U.S.C. §102(e) as being clearly anticipated by US Patent No. 6,728,265 ("Yavatkar et al."). Applicant respectfully requests reconsideration.

Claim 1 includes limitations not found in Yavatkar et al., including at least the following:

> a memory that stores data packets received by the first port, the memory being coupled to the first port and to the second port;
>
> a control circuit that manages the memory as a plurality of queues having respective priorities, including logic to place a packet received from the host into one of the plurality of queues according to a quality of service parameter associated with the packet, and logic to service packets in the plurality of queues according to the respective priorities; and
>
> logic to dynamically allocate space in said memory to the queues in the plurality of queues.

The Examiner takes the mistaken position that the FIFO memory 106 of Fig. 5 of Y corresponds with the "memory" recited in claim 1. The FIFO memory 106 of Fig. 5 of Y is in the receive path, and is not used by a control circuit that includes "logic to place a packet

received from the host..." as required in a claim 1. Rather, the FIFO memory 106 is used for placement of packets received from the network interface 90. Therefore, the Examiner's reliance on the FIFO memory 106 in the receive path of Fig. 5, as satisfying the claim limitation is mistaken.

With respect to the transmit path of Fig. 5 in Y, FIFO memory 122 in the transmit path of the controller and a buffer 410 of uncertain location are utilized for storing data of packets being transmitted, and could correspond to the "memory" recited in claim 1. See, Y column 5, line 50 through column 7, line 18. As discussed in Y, packets in the transmit path from the host are stored in "one or more FIFO memories 122..." (column 6, lines 14-15). Y also discusses a scheduler 400 (Fig. 5a) stating that it "may be a software entity", which operates on a higher priority and a lower priority queues 402, 404 (not labeled in Fig. 5a) by either causing transmission of the packet, or storing the data of the packet in a buffer 410 (labeled BETTER in Fig. 5a). The physical implementation and the location of the buffer 410 are not described.

There is no discussion in Y that suggests the limitation in claim 1 reading "logic to dynamically allocate space in said memory to the queues in the plurality of queues." The statement in Y that there are one or more FIFO memories 122, suggest that each of the priority queues have their own physical FIFO memory. Thus, there is no dynamic allocation of memory to the queues. The description of the operation of the buffer 410 suggests that it is used for storage of individual frames or packets after they have been removed from the queues. Therefore claim 1 is not anticipated by Y.

Accordingly, Y does not anticipate claim 1, and does not anticipate claims 2, 3 and 6-16 which depend therefrom, and reconsideration is respectfully requested.

With respect to claim 9 (and parallel claims 25 and 41), the Examiner takes the position that the driver program 57 dynamically allocates space in memory 100. As mentioned above, the memory 100 does not store packet data in the transmit path as required by the claim. Furthermore, the driver program 57 stores and remove "tuples" from the memory 100. A "tuple" is a data structure that defines a TCP/IP connection, as shown and Fig. 6 of Y, and is used for managing the received path of the network controller. The "tuple" does not relate to memory allocation on the network controller at all, and does not define a free buffer or a used buffer in a memory that stores packet data, as required by claim 9. It does not dynamically allocate space in a memory of the transmit path that stores packet data as required by claim 9.

With respect to claims 10-11 (and parallel claims 26-27 and 42-43), the Examiner takes the position that the "tuples" 140 in memory 100 are stored in noncontiguous memory, citing column 3, lines 3-7. This citation is apparently a typographical error. Nonetheless, there is no discussion in Y that suggests that the "tuples" are stored in noncontiguous memory. Furthermore, as mentioned above, the structures are not related to dynamic memory allocation to queues in a transmit path buffer, as required by these claims.

With respect to claims 12-13 (and parallel claims 28-29 and 44-45), the Examiner takes the position that the driver 57 maintains a list of free buffers and a list of used buffers, and refers again to the memory 100. As mentioned above, the memory 100 is unrelated to the transmit path queues. The Examiner also cites the queues 402 and 404 of Fig. 5a, as discussed at column 6, lines 31-50. The discussion in Y at column 6, line 31-50, relates to processing the queues based on a time stamp provided by the driver 57 for the purposes of maintaining a quality of service for lower priority queues. Allocation of memory to the queues is not discussed anywhere in the document.

With respect to claims 14-15 (and parallel claims 30-31 and 46-47), the Examiner cites direct memory access channels 304, and takes the position that a list of buffer descriptors for corresponding buffers in memory 100 is inherently maintained. The Examiner's reliance on inherency here is misplaced. As mentioned above, the memory 100 is unrelated to the transmit path as required by the claims herein. Furthermore, the buffer 304 in the direct memory access channels resides at the application layer as noted in Fig. 7 in the host computer, and not on the network controller 52. Finally, management of buffers can take on a wide variety of protocols, other than the use of free buffer and used buffer lists. Thus, even if the buffer 304 corresponded to the memory of claim 1, it is not "inherent" that it would be managed in the way claimed.

Independent method claim 17 is likewise limited to the transmit path, and requires dynamic allocation of space to the queues. The Examiner did not provide bases separate from that applied to claim 1, in support of the rejection of claim 17. Applicant submits that claim 17 is patentable for at least the reasons discussed above with respect to claim 1. Likewise, the claims 22-32 which are dependent from claim 17 are not anticipated by Y.

Independent claim 33 is directed to an integrated circuit including transmit path structures, along with "logic to dynamically allocate space... to the queues..." The Examiner did not provide bases separate from that applied to claim 1, in support of the rejection of claim 33.

Thus, applicant submits that claim 33, and claims 38-48 which depend therefrom, are not anticipated by Y.

Accordingly, reconsideration of the rejection of claims 1-3, 6-17, 22-33 and 38-48 is respectfully requested.

Allowable Subject Matter

The Examiner has objected to claims 2-6, 18-21 and 34-37 as being dependent upon a rejected base claim, but has indicated that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if no art rejection can be applied. Applicant does not amend such claims, in view of the arguments set forth above, that their respective base claims should be allowed

Accordingly, reconsideration of the objection to claims 2-6, 18-21 and 34-37 is respectfully requested.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (3COM 3715-1).

Respectfully submitted,

Dated: 25 May 05

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